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Future integration of metal-insulator-metal capacitors requires devices with high capacitance density and low quadratic voltage coefficient of capacitance (α). A major problem is that the increase in capacitance density is usually accompanied by increased voltage nonlinearities. By combining two high-k materials with opposite α, it is demonstrated that it is possible to obtain capacitors with both high capacitance density and minimal nonlinearity. A $SrTiO_3/ZrO_2$ bilayer was used to elaborate capacitors displaying a voltage coefficient of -60 ppm/V^2 associated with a density of 11.5 fF/μm^2. These devices constitute excellent candidates for the next generation of metal-insulator-metal capacitors. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3158951]

Capacitors are key passive components in most of the integrated circuits which are used in analog filtering, dc decoupling, and analog-to-digital conversion. Following the integration and component size reduction efforts, capacitors are meant to be integrated on-chip, within the back-end metallization levels. Getting small size capacitors with high capacitance values requires using dielectrics possessing a high capacitance density per unit area, i.e., high-κ dielectrics. Therefore, the traditional dielectrics, SiO_2 and Si_3N_4, were forsaken because of their low dielectric constant ($\kappa<10$) and there is a lot of ongoing effort to develop high-κ materials ($\kappa>15$) such as Ta_2O_5, HfO_2, and ZrO_2, to name a few.[1–10]

An important issue regarding capacitor performances is the voltage linearity, which shows the dependence of capacitance (C) on the applied bias (V). For high-κ oxides it is usual to observe a quadratic voltage dependence of capacitance, $[C(V)-C_0]/C_0=\alpha V^2+\beta V$, where C_0 is the capacitance at zero bias, and α and β are the quadratic and linear coefficients. For most of the high-κ dielectrics the coefficient α is in the 100–1000 ppm/V^2 range and the coefficient β is in the 100 ppm/V range.[1–11] As a consequence, for usual working voltages (1–3 V) the quadratic contribution prevails ($\alpha V^2>\beta V$) and the most important parameter that must be controlled is the quadratic coefficient α. Usually α is observed to increase dramatically with decreasing oxide thickness.[3,7,8,11] Thus, the effort to increase the capacitance density ($C_S=\kappa\varepsilon_0/t$) by decreasing the thickness (t) is always limited by a large increase of α. The difficulty to obtain both high C_S and low α can be quantified by introducing the ratio α/C_S^2. The reason for introducing C_S^2, instead of C_S, is the following. For practical applications the capacitance variation is written as a function of V, but physically $(C-C_0)/C_0$ should vary with the electric field ($E=V/t$), i.e., it should be independent of the oxide thickness. Rewriting $(C-C_0)/C_0$ as a function the electric field, $[C(E)-C_0]/C_0=\alpha E^2t^2+\beta Et$, it is seen that the relative capacitance variation does not dependent on the oxide thickness if α varies with $1/t^2$. In that case the ratio α/C_S^2 is also expected to be independent of the oxide thickness.[11] These ideas are summarized in Fig. 1 which shows α as a function of C_S for different materials. On this plot the ratio α/C_S^2 appears as a material's figure of merit which varies from 10 (ppm μm^2/V^2 fF^2) for materials such as HfO_2, down to one for oxides such as Ta_2O_5. According to the International Technology Roadmap for Semiconductors (ITRS),[12] in a few years application will require $\alpha<100$ ppm/V^2 and $C_S>10$ fF/μm^2. This is a difficult challenge which is better seen in Fig. 1 as a more general difficulty to get $\alpha/C_S^2<1$.

A way to reduce α was proposed by Kim *et al.*[1] It consists in using a bilayer capacitor where a dielectric (SiO_2) with a negative α is used to compensate the oxide (HfO_2) with a positive α. By using a 12 nm HfO_2/4 nm SiO_2 stack, these authors[1] obtained a very low α value of 14 ppm/V^2 and a α/C_S^2 ratio which is clearly below unity. However, the low κ value of SiO_2 prevented them to get high C_S values

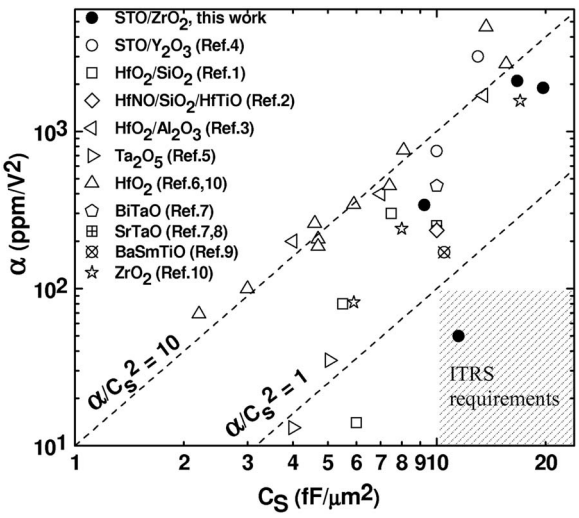

FIG. 1. Quadratic coefficient α as a function of capacitance density C_S for different materials of the literature. The figure of merit α/C_S^2 is expressed in ppm μm^2/V^{2}fF^2. The shaded area represents long term (2016) ITRS requirements (Ref. 12).

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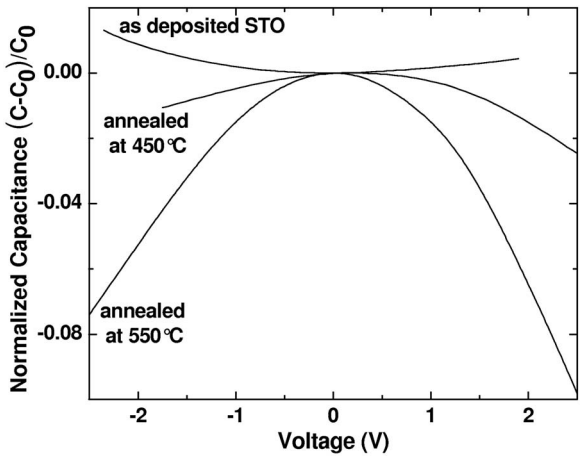

FIG. 2. Normalized capacitance vs bias for a 20 nm STO layer (as-deposited, annealed in air at 450 °C, and annealed in air at 550 °C).

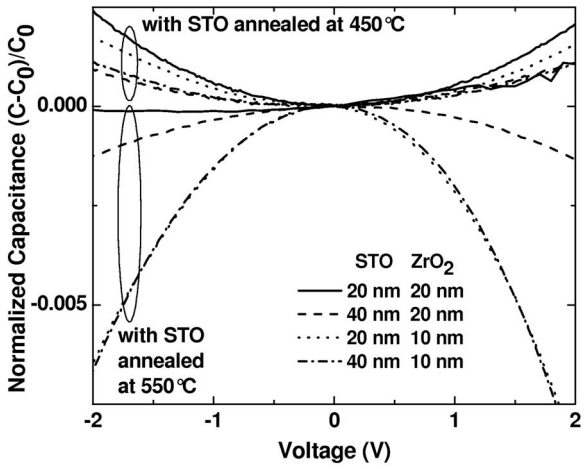

FIG. 3. Normalized capacitance vs bias for STO/ZrO_2 stacks. The stacks make use of STO annealed at 450 °C (upper curves) or at 550 °C (lower curves). Best performances are obtained with STO(550 °C, 20 nm)/ZrO_2(20 nm).

(6 $fF/\mu m^2$). Since then, other multilayer structures were investigated, but none of them were successful in getting $\alpha/C_S^2<1$ to fulfill roadmaps requirements (see Fig. 1).[3,4] In the present work we studied $SrTiO_3$ (STO)/ZrO_2 bilayers. ZrO_2 is a high-κ dielectric with positive α in the 100–1000 ppm/V^2 range[10] (Fig. 1). STO was chosen as a dielectric with a negative α to compensate for the ZrO_2 positive α coefficient. Contrary to SiO_2, STO can reach high-κ values (65 in this study) which allows to maintain an overall high capacitance density. By carefully engineering the STO/ZrO_2 thickness ratio it is demonstrated that STO/ZrO_2 capacitors provide $\alpha/C_S^2<1$ and appear as a solution to meet the long-term ITRS roadmap.

STO layers were deposited at room temperature by argon ion beam sputtering on Pt(100 nm)/TiO_2(10 nm)/SiO_2(500 nm)/Si substrates.[13] STO postannealings (1 h) were performed in air at 450 or 550 °C (as specified in the discussion). ZrO_2 layers were deposited on STO by metal-organic chemical-vapor deposition at 400 °C, in Ar/O_2 mixtures containing Zr(Obut)2(mmp)2 as a Zr precursor. Gold top electrodes were deposited by electron beam evaporation to form metal-insulator-metal (MIM) capacitors. *C-V* measurements were performed at 100 kHz using a HP4284 capacitance meter.

Figure 2 shows $[C(V)\text{-}C_0]/C_0$ for a 20 nm STO layer in three different states (as-deposited, annealed at 450 °C and annealed at 550 °C). As-deposited STO is in an amorphous state and displays a positive α(2200 ppm/V^2) and a quite low κ value of about 20. An annealing at 450 °C reverses the sign of the voltage coefficient (α=−3800 ppm/V^2). Still, the κ value of this annealed film remains low (20) indicating that crystallization is partial. Annealing at 550 °C further drives α toward negative values (−12 800 ppm/V^2) and allows to reach higher κ values (65). This demonstrates that the α value of STO layers can be tuned from positive values (as-deposited, amorphous layers) to negative values (air annealed, semicrystalline layers). Crystalline and stoechiometric STO is a paraelectric perovskite material which is known to display negative voltage coefficients.[14] The positive voltage coefficient measured for the amorphous films is probably due to the loss of the crystalline state, as well as oxygen deficiencies. Indeed, amorphous $BaTiO_3$ also has a positive voltage coefficient which decreases upon oxygen addition during deposition.[15] Moreover, oxygen vacancies are likely defects to be at the origin of nonlinearities observed in MIM capacitors.[16] Therefore, in amorphous dielectrics such as $SrTiO_3$ or $BaTiO_3$ (perovskite family) it is thought that oxygen vacancies control nonlinearities. Upon annealing in oxygen (air) the material crystallizes and recovers oxygen stoechiometry, leading to a "normal" negative voltage coefficient.[14]

Starting from STO layers with negative α, ZrO_2 layers were deposited on top of the STO films. Stacks with different STO and ZrO_2 thicknesses were tested (see Fig. 3 and Table I). The STO(20 nm)/ZrO_2(20 nm) bilayer is clearly the most interesting one in terms of performances. Corresponding α and C_S are −60 ppm/V^2 and 11.5 $fF/\mu m^2$ (figure of merit $\alpha/C_S^2=0.46<1$). These characteristics meet long-term ITRS requirements (Fig. 1). The dc leakage current was also measured and the values are shown in Table I. For the 20 nm/20 nm bilayer, the leakage current at 2 V is 3.5×10^{-8} A/cm^2, close to ITRS specifications ($<10^{-8}$ A/cm^2 at 1.8 V). The breakdown field of the 20 nm/20 nm stack was measured around 4 MV/cm (15 V across the capacitor). Since the κ value of ZrO_2 is three times lower than the STO one, most of the electric field is applied to the ZrO_2 layer, which supports higher breakdown electric fields (typically 5 MV/cm compared to 1 MV/cm for STO). It is also noted that the $(C(V)\text{-}C_0)/C_0$ curve is asymmetrical with respect to

TABLE I. Capacitance density, experimental quadratic coefficient, and theoretical quadratic coefficient calculated from Eq. (1), where ε(STO)=65, α(STO)=−12 800 ppm/V^2 (this work), $\varepsilon(ZrO_2)$=20, $\alpha(ZrO_2)$=+250 ppm/V^2 (Ref. 10), and leakage current of STO/ZrO_2 capacitors. STO was postannealed in air at 550 °C during 1 h.

Layers					
STO (nm)	ZrO_2 (nm)	C_S ($fF/\mu m^2$) at 100 kHz	α (ppm/V^2) Expt.	α (ppm/V^2) Theor.	I_S (A/cm^2) at 2 V
40	20	9	−350	−644	2.5×10^{-8}
40	10	16.5	−2280	−2153	2.7×10^{-8}
20	20	11.5	−60	−54	3.5×10^{-8}
20	10	19.5	−1900	−644	3.4×10^{-8}
20	⋯	29	−12 800	⋯	1×10^{-7}

the sign of V (20 nm/20 nm stack, STO annealed at 550 °C, Fig. 3). This can be explained by the importance of the linear coefficient $\beta(+143\ \text{ppm/V})$ which gives a linear contribution as important as the quadratic one. However, in practice the β coefficient has less importance because it can be more easily compensated by circuit design.[17] At 125 °C the characteristics worsen. The α coefficient increases to $-135\ \text{ppm/V}^2$. Though the characteristics are good at room temperature, studies are still needed to assess their thermal stability.

Low α values of the STO/ZrO_2 stacks can be explained as follows. Let us denote by C_1, t_1, κ_1, α_1, and β_1; the capacitance, the thickness, the dielectric constant, the voltage coefficients of the STO layer, and V_1 the voltage across this layer (correspondingly, C_2, t_2, κ_2, α_2, β_2, and V_2 for the ZrO_2 layer). The total capacitance C is $(C_1C_2)/(C_1+C_2)$ and the voltage across the stack is $V=V_1+V_2$. Calculation of α and as a function of α_1, α_2, β_1, and β_2 is made by writing $(dC/dV)=2\alpha C_0V+\beta C_0=2\alpha C_0(V_1+V_2)+\beta C_0$. We can also write $(dC/dV)=(\delta C/\delta C_1)(\delta C_1/\delta V)+(\delta C/\delta C_2)\times(\delta C_2/\delta V)$ and $(\delta C_1/\delta V)=(\delta V_1/\delta C_1+\delta V_2/\delta C_1)^{-1}=(\delta C_1/\delta V_1)(1+\delta V_2/\delta V_1)^{-1}$. Using $(\delta C_1/\delta V_1)=2\alpha_1C_{10}V_1+\beta_1C_{10}$ and the displacement field continuity at the interface $\kappa_1(V_1/t_1)=\kappa_2(V_2/t_2)$ (dC/dV) can now be expressed as a function of α_1, α_2, κ_1, and κ_2. Comparing with the expression of (dC/dV) as a function of α and β, one finds

$$\alpha=\alpha_1\left(\frac{1}{1+\frac{\kappa_1}{\kappa_2}\frac{t_2}{t_1}}\right)^3+\alpha_2\left(\frac{1}{1+\frac{\kappa_2}{\kappa_1}\frac{t_1}{t_2}}\right)^3, \tag{1}$$

$$\beta=\beta_1\left(\frac{1}{1+\frac{\kappa_1}{\kappa_2}\frac{t_2}{t_1}}\right)^2+\beta_2\left(\frac{1}{1+\frac{\kappa_2}{\kappa_1}\frac{t_1}{t_2}}\right)^2. \tag{2}$$

As explained in the introduction, we will focus on the quadratic coefficient α [Eq. (1)]. In this work we measured $\kappa_1=65$ and $\alpha_1=-12\,800\ \text{ppm/V}^2$ (see Table I). From Ref. 10 we consider $\kappa_2=20$ and $\alpha_2=+250\ \text{ppm/V}^2$. Reporting these values in Eq. (1) (with $t_1=20$ nm and $t_2=20$ nm) we get $\alpha=-54\ \text{ppm/V}^2$, which is very close to the experimental value of $-60\ \text{ppm/V}^2$. The experimental and the theoretical α also agree very well for the 40 nm/10 nm stack and are of the same order of magnitude for the 40 nm/20 nm and for the 20 nm/10 nm stacks (Table I). Thus, on average, Eq. (1) appears to predict the final voltage coefficient quite well (provided that the characteristics of individual layers are known).

To conclude, high performance MIM capacitors are obtained by combining two high-k materials with opposite quadratic voltage coefficient of capacitance. By adjusting the thickness of each layer [Eq. (1)], it is possible to minimize the quadratic voltage coefficient, while maintaining high capacitance density $(\alpha/C_S^2<1)$. This concept was applied to STO/ZrO_2 stacks, but it can be extended to other couples of dielectrics.

[1] S. J. Kim, B. J. Cho, M.-F. Li, S.-J. Ding, C. Zhu, M. B. Yu, B. Narayanan, A. Chin, and D.-L. Kwong, IEEE Electron Device Lett. **25**, 538 (2004).
[2] V. Mikhelashvili, P. Thangadurai, W. D. Kaplan, and G. Eisenstein, Appl. Phys. Lett. **92**, 132902 (2008).
[3] S.-J. Ding, H. Hu, C. Zhu, S. J. Kim, X. Yu, M.-F. Li, B. J. Cho, D. S. H. Chan, M. B. Yu, S. C. Rustagi, A. Chin, and D.-L. Kwong, IEEE Trans. Electron Devices **51**, 886 (2004).
[4] M. Kahn, C. Vallée, E. Defay, C. Dubourdieu, M. Bonvalot, S. Blonkowski, J. R. Plaussu, P. Garrec, and T. Baron, Microelectron. Reliab. **47**, 773 (2007).
[5] E. Deloffre, L. Montès, G. Ghibaudo, S. Bruyère, S. Blonkowski, S. Bécu, M. Gros-Jean, and S. Crémer, Microelectron. Reliab. **45**, 925 (2005).
[6] S. J. Kim, B. J. Cho, M. F. Li, X. Yu, C. Zhu, A. Chin, and D.-L. Kwong, IEEE Electron Device Lett. **24**, 387 (2003).
[7] L. Goux, H. Vander Meeren, and D. J. Wouters, J. Electrochem. Soc. **153**, F132 (2006).
[8] M. Lukosius, C. Wenger, S. Pasko, L. Costina, J. Dabrowski, R. Sorge, H. J. Mussig, and C. Lohe, IEEE Trans. Electron Devices **55**, 2273 (2008).
[9] Y. H. Jeong, J. H. Paik, Y. J. Lee, and S. Nabm, J. Electrochem. Soc. **155**, G214 (2008).
[10] S. Blonkowski, Appl. Phys. Lett. **91**, 172903 (2007).
[11] C. Durand, C. Vallée, C. Dubourdieu, M. Kahn, M. Derivaz, S. Blonkowski, D. Jalabert, P. Hollinger, Q. Fang, and I. W. Boyd, J. Vac. Sci. Technol. A **24**, 459 (2006).
[12] The International Technology Roadmap for Semiconductors (ITRS) (Semiconductor Industry Association, 2008), Table RFAMS3 On-Chip Passives Technology Requirements, http://www.itrs.net/Links/2008ITRS/Home2008.htm.
[13] E. Defaÿ, B. Andre, F. Baume, G. Tartavel, D. Muyard, and L. Ulmer, Ferroelectrics **288**, 121 (2003).
[14] See, for instance, C. Ang and Z. Yu, Phys. Rev. B **69**, 174109 (2004), and references therein.
[15] F. El Kamel, P. Gonon, and C. Vallée, Appl. Phys. Lett. **91**, 172909 (2007).
[16] P. Gonon and C. Vallée, Appl. Phys. Lett. **90**, 142906 (2007).
[17] D. Dornisch, G. Wilk, G. Li, K. M. Ring, D. J. Howard, and M. Racanelli, ECS Trans. **6**, 755 (2007).